MOTOROLA
SEMICONDUCTOR
3501 Ed Bluestein Blvd Austin TX 78721

MC14411

BIT RATE GENERATOR

The MC14411 bit rate generator is constructed with complementary MOS enhancement mode devices. It utilizes a frequency divider network to provide a wide range of output frequencies.

A crystal controlled oscillator is the clock source for the network. A two-bit address is provided to select one of four multiple output clock rates.

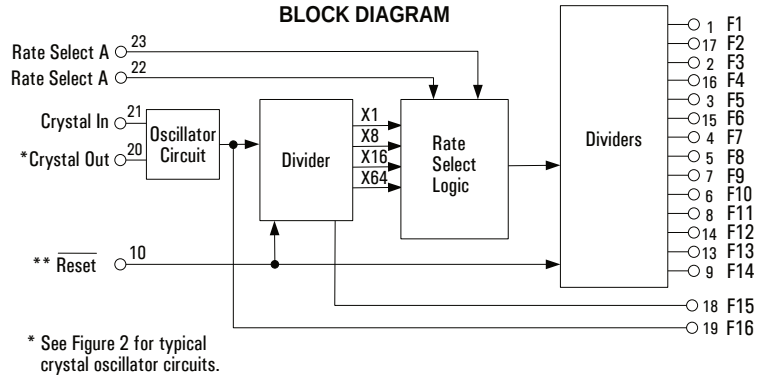
Applications include a selectable frequency source for the equipment in the data communications market, such as teleprinters, printers, CRT terminals and microprocessor systems.

- Single 5.0Vdc (± 5%) Power Supply
- Internal Oscillator Crystal Controlled for Stability (1.8432 Mhz)
- Sixteen Different Output Clock Rates
- 50% Duty Cycle
- Programmable Time Bases for One of Four Multiple Output Rates
- Buffered Outputs Compatible with Low Power TTL
- Noise Immunity = 45% of Vdd Typical
- Diode Protection on All Inputs
- External Clock may be applied to Pin 21
- Internal Pull-up Resistor on Reset Input

MAXIMUM RATINGS (Voltages referenced to Vss, Pin 12.)

Rating	Symbol	Value	Unit
DC Supply Voltage Range	Vdd	5.25 to - 0.5	V
Input Voltage, All Inputs	Vin	Vdd + 0.5 to Vss - 0.5	V
DC Current Drain Per Pin	I	10	mA
Operating Temperature Range	Ta	-40 to +85	°C
Storage Temperature Range	Tstg	-65 to +150	°C

BLOCK DIAGRAM



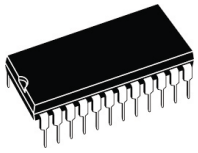
* See Figure 2 for typical crystal oscillator circuits.

** When Reset = 0, outputs F1 through F14 = 0, Outputs F15 and F16 = 1.

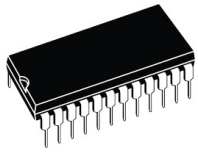
CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

BIT RATE GENERATOR

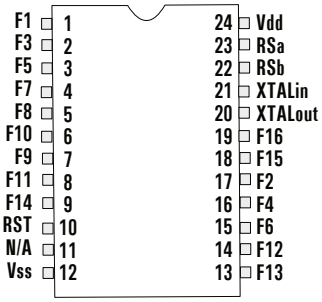


L SUFFIX
CERAMIC PACKAGE
CASE 623



P SUFFIX
PLASTIC PACKAGE
CASE 709

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and Vout be constrained to the range Vss ≤ (Vin or Vout) ≤ Vdd.

Tie unused inputs to appropriate logic levels

Characteristics	Symbol	V_{DD} V_{DC}	-40 °C		25 °C			85 °C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Supply Voltage	V_{DD}	--	4.75	5.25	4.75	5.0	5.25	4.75	5.25	V
Output Voltage "0" Level	V_{out}	5.0	--	0.05	--	0	0.05	--	0.05	V
"1" Level		5.0	4.95	--	4.95	5.0	--	4.95	--	V
Input Voltage										
(V_O = 4.5V or 5.0V)	V_{IL}	5.0	--	1.5	--	2.25	1.5	--	1.5	V
(V_O = 0.5V or 4.5V)	V_{IH}	5.0	3.5	--	3.5	2.75	--	3.5	--	V
Output Drive Current										
(V_{OH} = 2.5V) Source	I_{OH}	5.0	-0.23	--	-0.20	-1.7	--	-0.16	--	mA
(V_{OL} = 0.4V) Sink	I_{OL}	5.0	0.23	--	0.20	0.78	--	0.16	--	mA
Input Current										
Pins 21,22,23	I_{in}	--	--	±0.1	--	±0.00001	±0.1	--	±0.1	μA
Pin 10		5.0	--	--	-1.5	--	-7.5	--	--	μA
Input Capacitance	C_{in}	--	--	--	--	5.0	--	--	--	pF
Quiescent Dissipation	P_Q	5.0	--	2.5	--	0.015	2.5	--	15	mW
Power Dissipation **† (Dynamic plus Quiescent) (C_L = 15pF)	P_D	5.0			$P_D = (7.5mW/MHZ)\ f + P_Q$					mW
Output Rise Time ** T_f = (3.0 ns/pF) C_L + 25ns	t_{TLH}	5.0	--	--	--	70	200	--	--	ns
Output Fall Time ** T_f = (1.5 ns/pF) C_L + 47ns	t_{THL}	5.0	--	--	--	70	200	--	--	ns
Input Clock Frequency	f_{CL}	5.0	--	1.85	--	--	1.85	--	1.85	MHz
Clock Pulse Width	$t_{W(C)}$	--	200	--	200	--	--	200	--	ns
Reset Pulse Width	$t_{W(r)}$	--	500	--	500	--	--	500	--	nz

† For dissipation at different external capacitance (C_L) refer to the corresponding formula:

$$P_T = (C_L = P_D + 2.6 \times 10^{-3} (C_L - 15pF) V_{DD}^2 f$$

Where: P_T,P_D in mW, C_L in pF, V_{DD} in V_{dc} and f in MHz

** The formula given is for typical characteristics only.

Table 1 – Output Clock Rates

Rate Select B	Rate Select A	Rate
0	0	X1
0	1	X8
1	0	X16
1	1	C64

Output Number	Output Rates (Hz)			
	X64	X16	X8	X1
F1	614.4K	153.6K	76.8K	9600
F2	460.8K	115.2K	57.6K	7200
F3	307.2K	76.8K	38.4K	4800
F4	230.4K	57.6K	28.8	3600
F5	153.6K	38.4K	19.2K	2400
F6	115.2K	28.8	14.4k	1800
F7	76.8K	19.2K	9600	1200
F8	38.4K	9600	4800	600
F9	19.2K	4800	2400	300
F10	12.8K	3200	1600	200
F11	9600	2400	1200	150
F12	8613.2	2153.3	1076.6	134.5
F13	7035.5	1758.8	879.4	109.9
F14	4800	1200	600	75
F15	921.6K	921.6k	921.6k	921.6k
F16*	1.843M	1.834M	1.834M	1.834M

*F16 is buffered oscillator output

FIGURE 1 – DYNAMIC SIGNAL WAVEFORMS

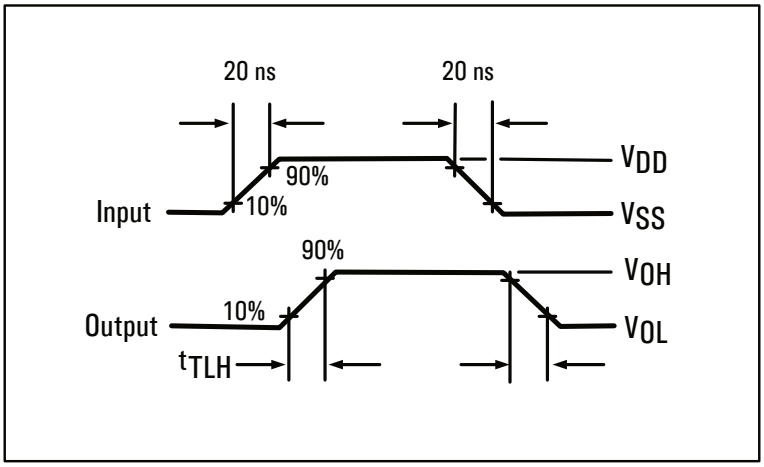
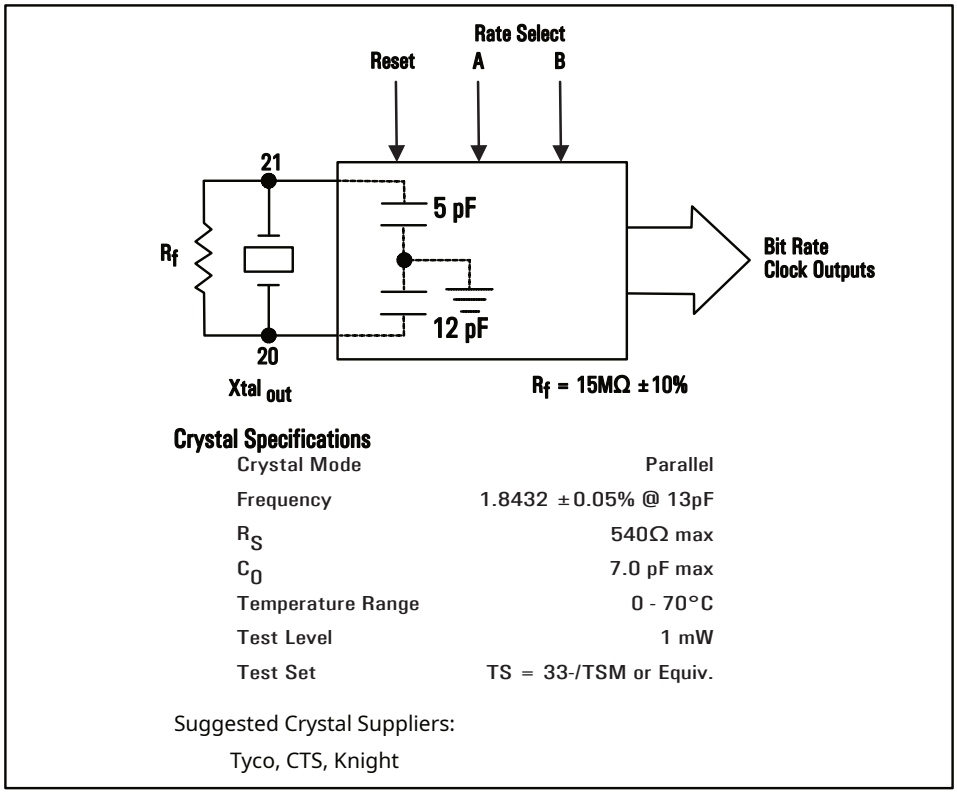


FIGURE 2 – TYPICAL CRYSTAL OSCILLATOR CIRCUIT

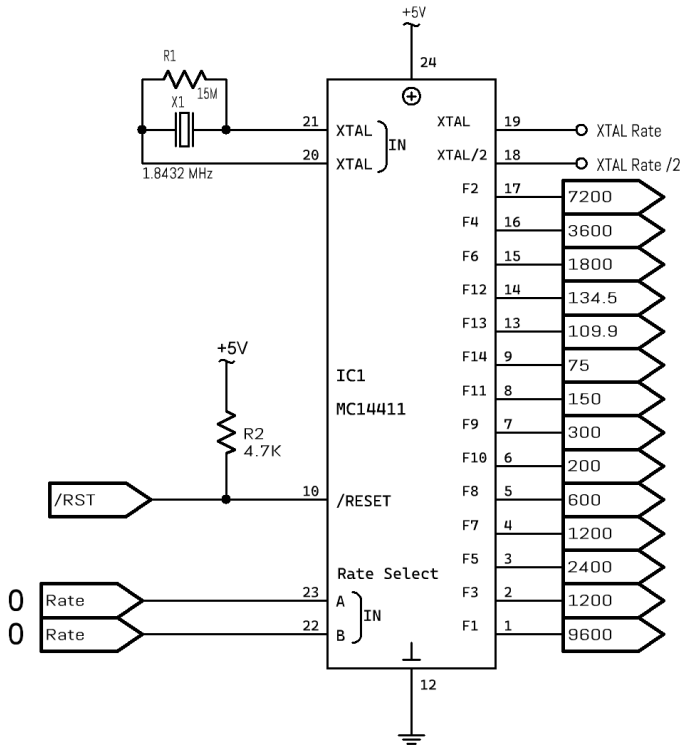


Crystal Specifications

Crystal Mode	Parallel
Frequency	1.8432 ±0.05% @ 13pF
R_S	540Ω max
C_0	7.0 pF max
Temperature Range	0 - 70°C
Test Level	1 mW
Test Set	TS = 33-/TSM or Equiv.

Suggested Crystal Suppliers:

Tyco, CTS, Knight



With X1 Rate setting (A&B LOW) Rates are shown.

This integrated circuit simultaneously generates 16 reference frequencies useful with serial interface clock speeds. In normal operation, pin 24 tied to +5V, pin 12 is tied to ground and pin 10 is tied to +5V through a pull-up resistor, allowing pin 10 to be pulled low for reset.

Pins 22 and 23 are used to program the the output frequencies based on the primary crystal frequency by providing various frequency divisions of 1X, 8X, 16X and 64X. The Baud Rate output frequencies are supplied on pins 1 through 9 and and 13 through 17. Each of these outputs can drive one TTL load or multiple CMOS loads.

The nominal frequency for the attached crystal is 1.8432 MHZ and is attached to pins 20 and 21 along with a bias resistor. The crystal frequency is output on pin 19 and this frequency divided by 2 is output on pin 18 and operate independently of the other frequency outputs. These outputs could be used to supply system clock, for example.

All outputs are symmetrical with 50% duty cycle.

Application Information

Typical applications of the Bit Rate Generator (BRG) include providing standard clock frequencies for data communications equipment, and external synchronization of a BRG output to a data source. The synchronization is accomplished by releasing the Reset input of the BRG during a data transition of the data source.

A typical data communication system is shown in Figure 3. In this example a standard frequency from the BRG is used for the clock input to the terminal transmitter and receiver (MC2257, MC2259). In a similar system the BRG, via Rate Select inputs, can provide up to 64 standard data communications frequencies, for a multiple frequency system. Some examples of equipment frequency requirements are shown in Table 2.

TYPICAL DATA COMMUNICATION
TERMINAL BLOCK DIAGRAM

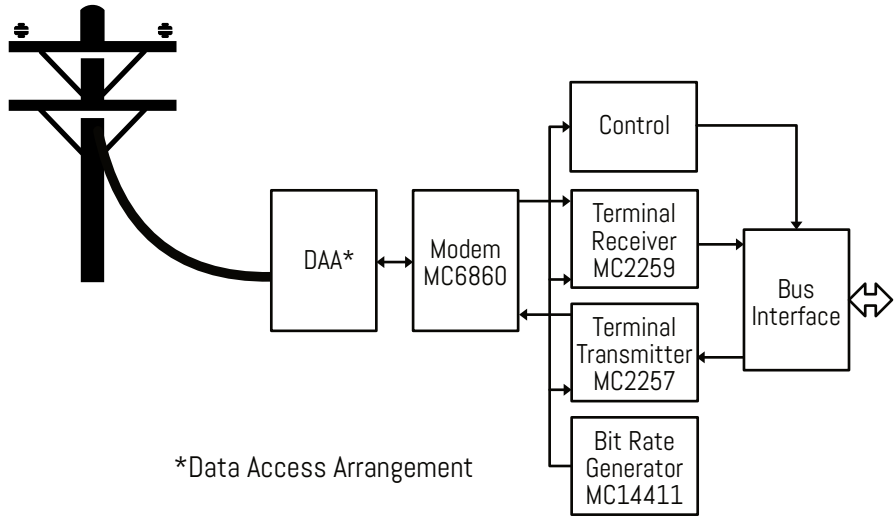


Table 2– Typical Data Communications Equipment Bit Rate Frequencies

Frequency (HZ)	Use
75 110 134.49 150 200 300	Asynchronous Mode Teleprinters Printers, typewriters CRT Terminals etc
600 1200	Asynchronous Mode (High Speed) Printers, typewriters Credit Card Verification CRT Terminals
2400 3600 4800 7200 9600	Synchronous Mode Computer to Computer Or Computer to Peripheral